What is claimed is:

1. A semiconductor involatile storage element which is a ferroelectric nonvolatile storage element including a field effect transistor:

wherein the field effect transistor includes a structure successively laminated with a first insulator layer, a first conductor layer, a ferroelectric layer and a second conductor layer on a channel region of a semiconductor substrate;

wherein the field effect transistor includes a third conductor and a fourth conductor respectively formed on a source region and a drain region on both sides of the channel region of the semiconductor substrate, further comprising:
a second insulator thin film between the third conductor and the fourth conductor and the first conductor layer.

2. The semiconductor nonvolatile storage element according to Claim 1:

wherein recesses and projections are included at a side wall of the first conductor layer opposed to the third and the fourth conductors and/or side walls of the third and the fourth conductors opposed to the first conductor layer.

3. The semiconductor nonvolatile storage element according to Claim 1 or 2:

wherein the semiconductor substrate is an SOI substrate.

4. The semiconductor nonvolatile storage element according to any one of Claims 1 through 3:

sub Al conc.

wherein an area of the second conductor layer above the ferroelectric layer is made smaller than an area of the ferroelectric layer.

5. The semiconductor nonvolatile storage element according to any one of Claims 1 through 4:

wherein the second conductor layer is disposed above an element isolating region of the semiconductor substrate.

6. The semiconductor nonvolatile storage element according to any one of Claims 1 through 5:

wherein each of the first insulator layer and the second insulator thin film comprises a layer of one material or a layer laminated with two or more of materials selected from a group consisting of SiO_2 (silicon oxide), SiN (silicon nitride), SiON (silicon oxynitride), SiO_2-SiN (ON film: silicon oxide - silicon nitride), SiO_2-SiN-SiO_2 (ONO film: silicon oxide - silicon nitride - silicon oxide), Ta_2O_5, $SrTiO_3$, TiO_2, (Ba,Sr)TiO_3, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, CeO_2, $CeZrO_2$ and YSZ (yttrium oxide stabilized zirconium oxide).

7. The semiconductor nonvolatile storage element according to any one of Claims 1 through 6:

wherein the ferroelectric layer is a layer of one material selected from a group consisting of $SrBi_2Ta_2O_9$, $PbTiO_3$, $PbZr_xTi_{1-x}O_3$, $Pb_yLa_{1-y}Zr_xTi_{1-x}O_3$, $Bi_4Ti_3O_{12}$, $SrNbO_7$, $Pb_5Ge_3O_{11}$ and $Sr_2Ta_xNb_{1-x}O_7$.

SUB B2

8. A method of fabricating a semiconductor nonvolatile

storage element which is a method of fabricating the semiconductor nonvolatile storage element according to Claim 1, said method comprising:

SUB B2

(a) a step of forming a dummy gate above a portion of a semiconductor substrate including a channel region;

(b) a step of integrally depositing a third and a fourth conductor above the semiconductor substrate and above the dummy gate;

(c) a step of flattening the third and the fourth conductors;

(d) a step of forming a source region and a drain region at the semiconductor substrate;

(e) a step of exposing the portion of the semiconductor substrate by removing the dummy gate;

(f) a step of forming an insulator thin film above the exposed portion of the semiconductor substrate, above side walls of the third and the fourth conductors and above the third and the fourth conductors;

(g) a step of successively laminating a first conductor layer, a ferroelectric layer and a second conductor layer above the insulator thin film; and

(h) a step of forming a structure laminated with the second conductor layer and the ferroelectric layer and the first conductor layer by patterning the second conductor layer, the ferroelectric layer and the first conductor layer.

9. A method of fabricating a semiconductor nonvolatile storage element which is a method of fabricating the semiconductor nonvolatile storage element according to Claim 1, said method comprising:

SUB B2

(a) a step of successively laminating a first insulator layer, a first conductor layer and an insulating layer for constituting a hard mask above a semiconductor substrate, a step of etching to form the insulating layer for constituting the hard mask, the first conductor layer and the first insulator layer in a predetermined pattern and a step of forming a source region and a drain region at the semiconductor substrate;

(b) a step of forming a second insulator thin film at side walls of the first insulator layer, the first conductor layer and the insulating film;

(c) a step of integrally depositing a third and a fourth conductor above the semiconductor substrate, above the insulating film, above the second insulator thin film and above a side wall of the second insulator thin film;

(d) a step of flattening the third and the fourth conductors;

(e) a step of forming an insulating layer above the third and the fourth conductors and a step of removing the insulating the film for constituting the hard mask;

(f) a step of successively laminating a ferroelectric layer and a second conductor layer above the insulating layer

above the third and the fourth conductors and above the first conductor layer; and

(g) a step of etching to form the second conductor layer and the ferroelectric layer by patterning the second conductor layer and the ferroelectric layer.

SUB B2

10. A method of fabricating a semiconductor nonvolatile storage element which is a method of fabricating the semiconductor nonvolatile storage element according to Claim 2, said method comprising:

(a) a step of successively laminating a first insulator layer, a first conductor layer and an insulating layer for constituting a hard mask above a semiconductor substrate, a step of etching to form the insulating layer for constituting the hard mask and the first conductive layer in a predetermined pattern and a step of forming a source region and a drain region at the semiconductor substrate;

(b) a step of forming recesses and projections at a side wall of the first conductor layer and a step of forming a second insulator thin film above the recesses and projections;

(c) a step of removing the first insulator layer above the source region and above the drain region;

(d) a step of integrally depositing a third and a fourth conductor above the semiconductor substrate, above the insulating film for constituting the hard mask, above the second insulator thin film and above a side wall of the second insulator

thin film;

(e) a step of flattening the third and the fourth conductors;

SUB B27

(f) a step of forming an insulating layer above the third and the fourth conductors;

(g) a step of removing the insulating film for constituting the hard mask;

(h) a step of laminating a ferroelectric layer and a second conductor layer above the insulating layer and the first conductor layer; and

(i) a step of etching to form the ferroelectric layer and the second conductor layer by patterning the ferroelectric layer and the second conductor layer.

11. The method of fabricating a semiconductor nonvolatile storage element according to Claim 10:

wherein the (h) step includes a step of laminating a barrier layer above the insulating layer and above the first conductor layer before the step of laminating the ferroelectric layer and in the (i) step, the barrier layer is also etched to form by patterning the barrier layer.

12. A method of fabricating a semiconductor nonvolatile storage element which is a method of fabricating the semiconductor nonvolatile storage element according to Claim 3, said method comprising:

(a) a step of successively laminating an insulating layer

and a dummy gate material above a semiconductor substrate, a step of etching to form the dummy gate and the insulating layer in a predetermined pattern and a step of forming a source region and a drain region;

Sub B2

(b) a step of integrally depositing a third and a fourth conductor above the semiconductor substrate and above the dummy gate and a step of flattening the third and the fourth conductors;

(c) a step of removing the dummy gate;

(d) a step of removing the insulating layer and forming recesses and projections at side walls of the third and the fourth conductors;

(e) a step of forming a first insulator layer above the semiconductor substrate and forming a second insulator thin film above the third and the fourth conductor layers and above the recesses and the projections of the side walls of the third and the fourth conductors;

(f) a step of successively laminating a first conductor layer and a ferroelectric layer and a second conductor layer above the first insulator layer and above the second insulator thin film; and

(g) a step of etching to form the second conductor layer, the ferroelectric layer and the first conductor layer by patterning the second conductor layer, the ferroelectric layer and the first conductor layer.